DELAY LOCKED LOOP

DESCRIPTION

Technical Domain And Prior Art

[0001]   The invention relates to a Delay Locked Loop (DLL).

[0002]   DLL loops are commonly used to put two clock signals into phase alignment, particularly in DRAM (Dynamic Random Access Memory) memories. DLL loops can then give very good synchronism between a clock external to the integrated circuit and an internal clock.

5   DLL loops are also used to precisely generate or measure a time delay, or to generate signal sampling clocks (see "*An Eight Channel 36GSample/s CMOS Timing Analyser*", Dan Weinlader, Ron Ho, Chih-Kong Ken Yang, Mark Horowitz, 2000 IEEE International Solid-Sate Circuits Conference).

[0003]   The invention is applicable to all domains mentioned above, and particularly

10   advantageously, to generation and measurement of delays in transceivers using the ultra wide band type communication technique.

[0004]   The schematic diagram for a DLL loop according to prior art is shown in Figure 1. The DLL loop comprises a delay line composed of n delay cells Ri (i = 1, 2, 3, ..., n-1, n) in series, a phase/frequency detector 1, a charge pump 2 and a loop filter 3. Each delay cell introduces a

15   delay Δt identical to delays in other cells. The delay Δt may be controlled by a signal that may be a voltage or a current. Each delay cell may be made from a differential pair. The delay variation Δt is then obtained by the variation of the polarisation current of the differential pair.

[0005]   The input and output of the delay line are applied to the phase/frequency detector 1. The phase/frequency detector 1 may be a simple phase comparator that compares phases of input and output signals of the delay line. The signal output from detector 1 controls the charge pump 2 that then generates a current that depends on the phase difference between the input and output signals of the delay line. This current is applied to the input of the loop filter 3 to be filtered. The filtered current output from the loop filter 3 is applied to the cells of the delay line to control the delay of the cells.

[0006]   The operating method of a DLL loop according to known art will now be described.

[0007]   A signal with period T is applied to the input of the delay line. When the DLL loop is stable, the input and output signals of the delay line are in phase. The delay between these two signals is then equal to T. Since all delay cells are identical, the delay added by a cell is equal to T/n. In addition to the clock signal applied to the input to the delay line, there are then n clock signals a_i ($i = 1, 2, 3, ..., n-1, n$), a signal a_i being offset by the time interval iT/n with respect to the clock signal applied to the input of the delay line. The different signals a_i can be used to measure a delay, generate a delay, synthesise a frequency signal, reconstruct signals, etc.

[0008]   One advantage of this type of structure is its low consumption. However, several disadvantages can be emphasised.

[0009]   Thus, generating a delay mT/n can lead to the use of a large number n of cells. For example, a delay of $13T/100$ ($m = 13$ and $n = 100$) will require the use of a hundred delay cells.

[0010]   Furthermore, the structure is limited in frequency by the minimum delay Tmin imposed by each elementary delay cell. When working at maximum frequency, it is impossible to generate a delay that is not an integer multiple of Tmin.

[0011]   The invention does not have these disadvantages.

Presentation Of The Invention

[0012]   The invention relates to a delay locked loop comprising a line of delay cells mounted

5   in series, a delay signal output by the loop being output from the output of one of the delay

cells, the input of the delay cells line being connected to a first input of a phase/frequency

detector, for which a second input is connected to an output from the delay cell. The delay loop

comprises control means capable of modifying the output from the delay cell connected to the

second input of the phase/frequency detector, at the rate of a clock signal when stimulated by

10   control information.

[0013]   The delay locked loop according to the invention can thus be used to modify the

number of delay cells seen by the phase/frequency detector. This modification produces an

elementary delay of each delay cell different from the elementary delay T/n obtained according

to prior art.

15   [0014]   As will become clearer in the remainder of the description, the delay of an elementary

delay cell may then be a fractional delay. It is thus possible to obtain a fractional DLL loop.

[0015]   A modification in the number of delay cells seen by the phase/frequency detector may

be made at every clock tick of the signal applied to the input of the delay line. This modification

may also be made at a lower frequency.

20   [0016]   The use of a number of delay cells lower than the total number of delay cells available

also has the advantage that it reduces consumption of the DLL loop. Furthermore, the maximum

working frequency is increased since this maximum frequency is inversely proportional to the

quantity N.Tmin, where N is the number of delay cells used and Tmin is the minimum delay input by an elementary delay cell.

Brief Description Of The Figures

5   [0017]   Other characteristics and advantages of the invention will become clearer after reading a preferred embodiment of the invention made with reference to the appended figures, wherein:

- Figure 1 shows a delay locked loop according to prior art;

- Figure 2 shows a delay locked loop according to a first embodiment of the invention;

- Figure 3 shows an example of a delay locked loop according to the first embodiment of

10   the invention;

- Figure 4 shows a delay locked loop according to a second embodiment of the invention;

- Figures 5a and 5b respectively show an improvement to the delay locked loop according to the first embodiment of the invention and an improvement to the delay locked loop

15   according to the second embodiment of the invention.

[0018]   The same references denote the same elements in all figures.

Detailed Description Of Embodiments Of The Invention

[0019]   Figure 1 has already been described; therefore there is no point in describing it again.

20   [0020]   Figure 2 shows a delay locked loop according to a first embodiment of the invention.

[0021]   Apart from the elements already mentioned in the description in Figure 1, a DLL loop according to the first embodiment of the invention comprises multiplexing means 4. The

multiplexing means 4 comprise n signal inputs, one signal output, one clock input and one control input.

[0022]   Each signal input of the multiplexing means 4 is connected to a different delay signal ai (i = 1, 2, ..., n). The signal output is connected to one of the inputs of the phase/frequency

5   detector 1. The signal applied to the input of the phase/frequency detector 1 among the signals applied to the input of the multiplexer, is determined by a clock signal H applied to the clock input and by information I applied to the control input. At each tick of the clock signal H, the signal applied to the phase/frequency detector is chosen as a function of the information I. The information I thus selects the sequence of signals that are applied to the input of the

10   phase/frequency detector, at the rate of the clock signal H.

[0023]   The clock signal H may be the same signal as the clock signal applied to the input of the delay line, or it may be a different clock signal. The information I may be periodic or non-periodic information.

[0024]   In general, the number of delay cells seen by the phase/frequency detector can change

15   at each clock tick of the clock signal H or at a lower frequency. This modification may be applied such that the average value of the number of delay cells seen by the phase/frequency detector is chosen in advance as a function of the required fractional delay. For example, the average value of the number of delay cells seen by the detector may be obtained by taking a weighted average and using the number of clock ticks of the clock H during which the number

20   of delay cells is effective, as weighting for each delay cell. In this case there is a relation between the average number NC of delay cells used and the delay Δt of an elementary cell, namely:

$$\Delta t = T/NC$$

[0025] We will now describe a non-limitative example as an illustration of the performances

5   of a DLL loop according to the invention. We will consider a delay line that comprises ten delay

cells (n = 10). It is assumed that the clock H that controls multiplexing is identical to the clock

that is applied to the input of the delay line, except for a delay. The signal applied to the

phase/frequency detector is different from the input frequency at each clock tick. In this

example, it is also assumed that the signal selected by the information I to be applied to the

10   input of the phase/frequency detector is an alternation of signals a10 and a9. The average phase

that is compared by the phase/frequency detector is then equal to 9.5 Δt, where Δt is the delay of

one elementary cell. Therefore, we obtain the relation:

$$\Delta t = 2T/19$$

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[0026] It is then possible to generate delays equal to 2T/19, 4T/19, ..., 18T/19 with a line of

ten delays. Nineteen delays would be necessary to obtain the same result using a DLL loop

according to prior art.

[0027] We will now describe more generally how to generate any delay starting from a simple

20   fractional DLL loop. A simple fractional DLL loop means a DLL loop that only uses two

successive delay signals, for example signals an-1 and an, for multiplexing.

[0028]   It is assumed that signals an-1 and an are used during p clock ticks and q-p clock ticks respectively. The average value of the delay added by the delay line is then equal to $(n-p/q)\Delta t$. The value of the delay of an elementary cell is then given by the relation:

5

$$\Delta t = q \, T/(qn-p)$$

[0029]   Therefore as a non-limitative example, for a delay line comprising ten delay cells and assuming that I is a periodic signal with period 100T ($q = 100$ and the average value of a delay is then obtained on 100 points), the result is then:

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$$\Delta t = 100T/(1000-p)$$

[0030]   An evaluation of the number p then gives:

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$$P = PART[1000-100T/\Delta t]$$

where PART[X] represents the integer part of X.

[0031]   To make a fractional delay equal to aT/b at the output from the rank k delay cell, in which a and b are two arbitrary integer numbers, we need to set:

20

$$k \, \Delta t = a \, T/b, \text{ namely}$$

$$a \, T/b = k \, q \, T/(q \, n-p)$$

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[0032]   Therefore, the result is a system of 2 equations with 4 unknowns p, q, n and k, each

unknown being an integer number. There are always solutions to a system of equations like this.

[0033]   For example, to obtain a delay equal to 13T/100, the solution is as follows:

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$$p = 4, q = 13, n = 8, k = 1$$

[0034]   The delay 13T/100 is then obtained with only eight delay cells. This result should be

compared with the result obtained according to prior art in which 100 delay cells are necessary

(see above).

10   **[0035]**   Another example could be given for obtaining a delay of 14T/121. The following

solution is then obtained:

$$p = 5, q = 7, n = 18, k = 2$$

15   **[0036]**   In this example, the number of cells could be even further reduced by the following

solution:

$$p = 5, q = 14, n = 9, k = 1$$

20   **[0037]**   In this case nine cells are advantageously sufficient.

[0038]   An example of the DLL loop according to the first embodiment of the invention will

now be described with reference to Figure 3.

[0039]   According to the example in Figure 3, the multiplexing means 4 comprise a

multiplexer 5 and a sigma delta modulator 6. The sigma delta modulator 6 comprises a clock

input and a signal input. The clock signal H is applied to the clock input and the information I is

applied to the signal input. The sigma delta modulator 6 converts the information I into a digital

control signal C, at the rate of the clock signal H. The digital control signal C controls switching

of the multiplexer 5. One example of the use of a sigma delta modulator is that it reduces the

5   noise of the switching control information.

[0040]   For example, in the case of a simple fractional DLL loop, the information I applied to

the sigma delta modulator to generate a correct sequence of signals to be applied to the

phase/frequency detector, is equal to a fractional value p/q, as mentioned above. The signal C

output from the modulator may be in two different states (a +1 state to choose the signal an and

10   a 0 state to choose the signal an-1) such that the average value of signal C is equal to p/q, except

for the quantification error (however, this quantification error can be reduced by optimising the

modulator). It is then possible to obtain an average loop delay equal to the quantity (n-p/q) Δt,

which is the objective.

[0041]   A DLL loop according to the first embodiment of the invention is obviously not

15   limited to the example of the simple fractional DLL loop mentioned above. More generally, the

use of a sigma delta modulator with a multibit quantifier results in a choice between n delay

outputs from the DLL loop, where n is a number equal to or greater than 2.

[0042]   It is also possible according to the invention to apply variable information I to the

input of the sigma delta modulator. The result is then a delay or frequency modulated by a

20   variable magnitude contained in the information I. The number NC of delay cells used is then a

variable magnitude that modulates the delay Δt of an elementary cell. The invention can thus be

used to generate a variable delay used to generate a PPM (Pulse Position Modulation) signal

used in the UWB (Ultra Wide Band) technology.

[0043]   Figure 4 shows a second embodiment of a delay locked loop according to the
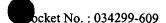
invention.

5   [0044]   Apart from the circuits shown in Figure 1, the delay locked loop in Figure 4 comprises

a first set of switches Iqi (i=1, 2, …, n), a second set of switches Ipi (i=1, 2, …, n) and a control

circuit 7. Each switch Ipi is placed at the output from the delay Ri and each switch Iqi is placed

in parallel with the assembly formed by the delay Ri and the switch Ipi.

[0045]   The switches Ipi and Iqi are controlled by control signals pi and qi respectively. The

10   control circuit 7 comprises a clock input and a control input on which a clock signal H and a

control signal I respectively are applied. The signals pi and qi are output from the control circuit

7. At each tick of the clock H, the control circuit 7 outputs a combination of control signals pi,

qi capable of opening or closing the corresponding switches Ipi, Iqi. It is then possible to

subtract one or several arbitrary delays from the delay loop. If the output from the delay loop

15   has to oscillate, for example between signals an and an-1, it is then possible to alternately short

circuit each of the delay cells using an algorithm adapted to this purpose (random algorithm,

noise formatting algorithm, etc.). This advantageously reduces the influence of the dispersion in

delays between each delay cell. For example, in the case in which the delay of the last delay cell

Rn is significantly different from the delay of the other cells, the influence of this cell will be

20   different from the influence of the other cells due to its switching external to the loop.

[0046]   A delay locked loop according to the second embodiment of the invention has the

same advantages as a delay locked loop according to the first embodiment. As a non-limitative

example, it is thus possible to make a simple fractional DLL loop using two successive delay signals, for example signals an-1 and an. The value of the delay Δt of an elementary cell is then given by the relation:

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$$\Delta t = q\ T/(qn-p),$$

where magnitudes p, q, n and T are the previously defined magnitudes.

[0047] Similarly, the control circuit 7 may be composed of a sigma delta modulator and a digital control signal (not shown on the figures). The clock signal H and the control signal I are

10 applied on the sigma delta modulator and a digital control signal C output by the sigma delta modulator is applied to the digital control circuit.
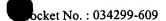
[0048] According to one improvement to the second embodiment of the invention, switches and switchable loads can be added at the input and output of the different delay cells such that the number of switches passed through is always the same regardless of the programmed delay,

15 and each delay cell always sees the same load on its input and on its output.

[0049] Within the context of making a delay locked loop using the silicon technology, and regardless of the embodiment of the invention, the precision of the generated delay or the synthesised frequency depends on the matching that exists between the different delay cells. The number of delay cells in a locked loop according to the invention is significantly lower than

20 the number of delay cells in a locked loop according to prior art, therefore the propagation time constraint for an elementary delay cell can be reduced. It is then possible to increase the surface

area of components used to make an elementary delay cell, which advantageously increases the precision of the loop.

[0050] Similarly, regardless of its embodiment, a delay locked loop according to the invention can advantageously be used to generate delays that are not integer multiples of the minimum

5 time Tmin, while working at the maximum working frequency.

[0051] In general, the large number of degrees of freedom in a DLL loop according to the invention compared with the number of degrees of freedom in a DLL loop according to prior art makes it possible to extend and very significantly improve loop performances.

[0052] The invention is advantageously made using conventional VLSI silicon integration

10 techniques.

[0053] Figures 5A and 5B show an improvement to the phase locked loop according to the first embodiment and the second embodiment respectively of the invention.

[0054] The operation of a delay locked loop includes two distinct phases: a latching phase and a phase during which the elementary time no longer varies.

15 [0055] The delay generated by each cell in the delay loop has a lower limit and an upper limit. A convergence problem can then arise during the latching phase, particularly when latching constraints are severe. This convergence problem may also arise due to the large dispersion of elementary times of the different cells when the delay locked loop is made using the silicon technology. A delay locked loop can then be in a locked state during the latching phase, when

20 the minimum delay of each cell is reached and the global delay is still too high. The delay locked loop according to the improvement to the invention represented in Figures 5A and 5B eliminates this disadvantage.
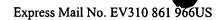
[0056]   According to the improvement to the invention, the delay locked loop comprises a

convergence analysis device 8, a switch 9 and a processing circuit 10, in addition to the

elements described above. The input to the convergence analysis device 8 is connected to the

output from the phase/frequency detector 1. The switch 9 comprises two signal inputs, a control

5   input and an output. A first input to the switch signal 9 is connected to the output from the

convergence analysis device 8 while the information I mentioned above is applied to the second

signal input. The output from switch 9 is connected to the input to the processing circuit 10, the

output from which is connected to the control input of the multiplexing means 4 (case in Figure

5A) or to the control input of the control circuit 7 (case in Figure 5B).

10   [0057]   The convergence analysis device 8 outputs information on its output that measures the

stability and convergence state of the loop. The convergence analysis device 8 also outputs the

control signal of switch 9.

[0058]   During the latching phase, the switch 9 is controlled such that the output from the

convergence analysis device 8 is connected through the processing circuit 10 to the control

15   input of the multiplexing means 4 (case in Figure 5A) or to the control input of the control

circuit 7 (case in Figure 5B). The processing circuit 10 uses convergence information output

from the device 8 to notify the multiplexing means 4 or the control circuit 7 whether it should

increase or reduce the number of cells in the loop. The signal S output from the processing

circuit 10 then constitutes a control used to select a number of delay cells that can prevent the

20   loop from getting locked.

[0059]   When the latching phase is complete, the switch 9 is controlled such that the input of

the processing circuit 10 is connected to the information I mentioned above. The information I

is then processed by the circuit 10 as a function of the number of delay cells selected during the

latching phase. Therefore, the processing circuit 10 will previously have memorised the number

of cells selected to obtain convergence. The signal S applied to the control input of the

multiplexing means 4 (case in Figure 5A) or the control input of the control circuit 7 (case in

5   Figure 5B) is then obtained starting from information I and the number of memorised cells.